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**TITLE:** GROUND PAD STRUCTURE FOR PREVENTING SOLDER  
EXTRUSION AND SEMICONDUCTOR PACKAGE HAVING THE  
GROUND PAD STRUCTURE

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## **GROUND PAD STRUCTURE FOR PREVENTING SOLDER EXTRUSION AND SEMICONDUCTOR PACKAGE HAVING THE GROUND PAD STRUCTURE**

### **BACKGROUND OF THE INVENTION**

#### **1. Field of the Invention**

This invention relates to a ground pad structure for preventing solder extrusion and a semiconductor package having the ground pad structure, and more particularly, to a surface mount technology that can be used in a flip-chip ball grid array (FCBGA) package structure to enhance the bonding reliability of the chip by modifying the formation of the ground ball pads.

#### **2. Description of Related Art**

A semiconductor chip is capable of being electrically connected to a substrate or a printed circuit board through a plurality of conductive metal solder means, such as solder balls or solder bumps being arranged in a matrix array, and is thereby packaged into a semiconductor package, such as a ball grid array (BGA) package, in a manner of the flip-chip formation.

The surface of the substrate is covered with an insulative solder mask layer while the chip is mounted in a flip-chip manner onto the substrate. A plurality of conductive traces are buried beneath the solder mask layer and a solder pad is formed on the terminal of each conductive trace at a location that corresponds to one of the solder bumps to be soldered on the chip and is exposed from the solder mask layer. As a result, after the solder bumps are bonded to the corresponding solder pads on the substrate, respectively, the electronic signals of the chip are capable of being transmitted to the

substrate and being electrically coupled to an external means (e.g. a printed circuit board) through the solder bumps and the conductive traces, which are distributed on the substrate and penetrate the resin core of the substrate through vias.

The terminal of the conductive trace (i.e. solder pad) is generally a solder mask defined (SMD) solder pad as shown in FIGS. 1A and 1B, wherein the size of the opening 102a of the solder mask layer 102 is smaller than the solder pad 103 formed on the resin core 100 of the substrate 10, so as to have the circumference of the solder pad 103 being covered by the solder mask layer 102.

Regarding the flip-chip packaging technology, a plurality of metal solder means 112 (in general, solder bumps) are pre-disposed onto the chip pads 113 on the active surface 110 (the surface distributed with a plurality of electric circuits and elements) of the chip 11, then the chip 11 is bonded and reflowed onto the substrate 10 with its active surface 110 facing downwardly to form a solder bonding portion including the chip pads 113, solder bumps 112 and solder pads 103, as shown in FIGS. 2A and 2B. An insulative material 12, such as resin, is thereafter filled into the gap under the chip 11 through an underfill or molding process to strengthen the solder joint of the solder bumps 112.

However, while the flip-chip structure has been encapsulated and proceeded with a followed reflow process for planting the solder balls, the solder bumps 112 within the solder bonding portion are molten and expanded in volume due to the high reflow temperature. As the space receiving the solder bumps 112 is surrounded by the insulative encapsulant 12, the molten and swelled solder bumps 112 are forced to be extruded and penetrated into the gaps between the solder mask layer 102 and the solder pads 103 and between the solder mask layer 102 and the resin core 100. As a result, bridges 105 or 106 cause an electric short between the adjacent solder bumps 112 or

between the adjacent conductive traces 101, as shown in FIGS. 2A and 2B. This is due to poor adhesion between the solder mask layer 102 and the solder pads 103 and thereby results in an easy penetration into the gap between the solder mask layer 102 and the solder pads 103 by the molten and extruded solder bumps 112. Although the adhesion between the solder mask layer 102 and the resin core 100 is better than that between the solder mask layer 102 and the solder pads 103, if the adhering area between the solder mask layer 102 and the resin core 100 is not large enough, the adhesion between the solder mask layer 102 and the resin core 100 would remain poor and results in an easy penetration into the gap between the solder mask layer 102 and the resin core 100 by the molten and extruded solder bumps 112 and contribute to the bridges occurred between the adjacent solder bumps 112 or between the adjacent conductive traces 101.

In comparison with the solder mask defined (SMD) solder pad, a non-solder mask defined (NSMD) solder pad is shown in FIGS 3A and 3B, wherein the opening 102b of the solder mask layer 102 is larger than the solder pad 103 formed on the resin core 100, and thereby expose the solder pad 103, a portion of the surface of the resin core 100 surrounding the solder pad 103, and a portion of the conductive trace 101 connecting the solder pad 103 together from the opening 102b of the solder mask layer 102.

While adopting the non-solder mask defined (NSMD) solder pad into a flip-chip ball grid array (FCBGA) package structure, as shown in FIG 4, the solder bump 112 is capable of being planted onto the solder pad 103 without contacting the solder mask layer 102 and result in a direct mounting between the surface of the resin core 100 exposed around the solder pad 103 and the insulative encapsulant 12. Since the adhesion between the insulative encapsulant 12 and the resin core 100 is good, the molten and swelled solder bumps 112 due to the high reflow temperature during the reflow process for planting the solder balls will have difficulty to extrude into the gap between the solder mask layer 102 and the resin core 100 through the gap between the

resin core 100 surrounding the solder pad 103 and the insulative encapsulant 12. As a result, bridges occurred between the adjacent solder bumps 112 or between the adjacent conductive traces 101 are prevented.

However, among a typical layout of the solder bumps within a flip-chip ball grid array (FCBGA) package, the ground solder bumps 112a are generally disposed in a central region and are mounted onto a ground plane 108 disposed on a corresponding location on the resin core 100 of the substrate 10. Under this layout, in order to create a non-solder mask defined (NSMD) ground pad on a location corresponding to the ground solder bump 112a on the ground plane 108, as shown in FIG 6, a pair of semi-circular slots 108a are formed respectively on the ground plane 108 to have the non-solder mask defined ground pad 108b be connected to the ground plane 108 through a pair of tie bars 108c, and the ground pad 108b and a portion of the tie bars 108c are thereby exposed together from the opening 102b (as shown in a dotted line in FIG 6) of the solder mask layer 102. However, the non-solder mask defined ground pad 108b is not only time-consuming in its fabrication, but also leads to a poor grounding ability since the non-solder mask defined ground pad 108b is connected to the ground plane 108 merely by a pair of tiny tie bars 108c. Moreover, the formation of a plurality of paired semi-circular slots 108a on the ground plane 108 will make the ground plane 108 an imperfect and non-continuous plane and will therefore dramatically affect the grounding ability of the ground plane 108.

As a result, the non-solder mask defined ground pad 108b as shown in FIG 6 is generally refrained from being provided onto the ground plane of the flip-chip ball grid array package. Instead, the solder mask defined (SMD) solder pad is adopted to maintain a perfect plane, as shown in FIGS. 5A and 5B, in order to achieve a preferred grounding ability.

However, although a good grounding ability is able to be maintained preferably by adopting the solder mask defined (SMD) solder pad on the flip-chip ball grid array package as shown in FIGS. 5A and 5B, an easy occurrence of electric shorts among the conductive traces due to the molted solder bump extruded and flooded over the adjacent conductive traces from the solder mask defined (SMD) solder pad is still inevitable. That is, as shown in FIGS. 5A and 5B, while the reflow process for planting the solder balls has been conducted, the ground solder bumps 112a located on the circumference of the ground plane 108 are molten and expanded in volume due to the high reflow temperature and are forced to be extruded and penetrated into the gaps between the solder mask layer 102 and the ground plane 108 due to poor adhesion therebetween. As a result, bridges 107 cause an electric short between the adjacent conductive traces 101, as shown in FIGS. 5A and 5B.

#### SUMMARY OF THE INVENTION

It is therefore an objective of this invention to provide a ground pad structure for preventing solder extrusion and a semiconductor package having the ground pad structure, which is capable of maintaining a good grounding quality and diminishing the occurrence of the electrical bridging among the adjacent conductive traces.

In accordance with the foregoing and other objectives, the invention proposes a ground pad structure for preventing solder extrusion, which comprises a ground plane made of conductive materials and covered by an insulative layer, such as an insulative solder mask layer, and a plurality of ground pads that are exposed from the solder mask layer are provided on the ground plane in locations corresponding to a plurality of ground conductive metal solder means, such as solder balls or solder bumps, soldered on a semiconductor chip, wherein, the ground pads located along the circumference of the ground plane are formed in a non-solder mask defined manner.

The invention also proposes a semiconductor package having a ground pad structure for preventing solder extrusion, which comprises the following constituent parts: a substrate having an insulative dielectric layer, a plurality of conductive traces disposed above and beneath the dielectric layer, and an insulative layer, such as an insulative solder mask layer, covering the conductive traces and the dielectric layer and having a plurality of openings, in which a plurality of non-ground pads are respectively formed on each terminal of the conductive traces and are exposed from the openings; a ground pad structure comprising a ground plane made of conductive materials and covered by the insulative layer, and a plurality of ground pads that are exposed from the openings of the insulative layer being provided on the ground plane, in which the ground pads located along the circumference of the ground plane being formed in a non-solder mask defined manner; a semiconductor chip with an active surface and a corresponding inactive surface, the active surface being formed with a plurality of non-ground conductive metal solder means and ground conductive metal solder means and being soldered to the substrate; an encapsulant body encapsulating the semiconductor chip, the conductive metal solder means, the surface of the insulative layer, and a portion of the surface of the dielectric layer; and a plurality of conductive elements, such as solder balls, planted under the substrate.

Since the ground pad structure of the present invention is capable of keeping the ground plane as a complete and continuous plate-shaped plane, an excellent grounding ability is thereby well maintained. In the meantime, while the ground pads located along the circumference of the ground plane being formed in a non-solder mask defined manner, the occurrence of unfavorable shorts due to the electrical bridging among the adjacent conductive traces can be avoided as the extrusion of the molten solder bumps from the ground pads located along the ground pad structure's circumference toward their adjacent conductive traces is effectively prevented.

## BRIEF DESCRIPTION OF DRAWINGS

The invention can be more fully understood by reading the following detailed description of the preferred embodiments, with reference made to the accompanying drawings, wherein:

FIGS. 1A-1B (PRIOR ART) are schematic elevated and sectional diagrams used to depict a conventional solder mask defined (SMD) solder pad;

FIGS. 2A-2B (PRIOR ART) are schematic sectional diagrams used to depict a flip-chip semiconductor package adopting the conventional solder mask defined (SMD) solder pad;

FIGS. 3A-3B (PRIOR ART) are schematic elevated and sectional diagrams used to depict a conventional non-solder mask defined (NSMD) solder pad;

FIG. 4 (PRIOR ART) is a schematic sectional diagram used to depict a flip-chip semiconductor package adopting the conventional non-solder mask defined (NSMD) solder pad;

FIGS. 5A-5B (PRIOR ART) are a schematic sectional diagram used to depict a flip-chip semiconductor package adopting a conventional ground pad structure and a schematic elevated sectional diagram according to the cutting line A-A shown in FIG. 5A;

FIG. 6 (PRIOR ART) is a schematic elevated diagram used to depict a ground plane adopting the conventional non-solder mask defined (NSMD) solder pad;



FIG. 7 is a schematic elevated diagram of an embodiment of a ground pad structure for preventing solder extrusion according to the present invention;

FIG. 8 is a schematic sectional diagram of an embodiment of a semiconductor package having the ground pad structure for preventing solder extrusion according to the present invention; and

FIG. 9 is a schematic elevated sectional diagram according to the cutting line B-B shown in FIG. 8.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the ground pad structure for preventing solder extrusion and the semiconductor package having the ground pad structure of the invention are disclosed in full details in the following with reference to FIGS. 7-9. However, instead of showing a real operative scheme in detail, the drawings depicting the embodiments illustrate merely the constituent parts related to the embodiments. It is to be noted that the semiconductor package of the invention will be more complex in its whole layout and with more details in the size and number of its components while in the real operative scheme.

Referring to FIG.7, the ground pad structure 200 for preventing solder extrusion of the invention comprises a ground plane 208 that is made of conductive materials, and the shape of the ground plane 208 may be formed in a square as shown in FIG. 7 or any other preferred shape to fit a given occasion. The ground plane 208 is to be provided on an insulative dielectric layer 100 of a substrate 10 and covered by an insulative layer 102, such as an insulative solder mask layer, as shown in FIG. 8, and a plurality of

ground pads 203, which are shown in dashed lines in FIG. 7, are provided on the ground plane 208 in locations corresponding to a plurality of ground conductive metal solder means 112a, such as solder balls or solder bumps, and are soldered on a semiconductor chip 11. The layout of the ground pads 203 may be arranged in a matrix array as shown in FIG. 7 or any other preferred layout to fit a given occasion. It is a characteristic feature of the invention that the ground pads 203 located along the circumference of the ground plane 208 are formed in a non-solder mask defined manner. That is, the ground pads 203 located along the circumference of the ground plane 208 are protruded from the circumference of the ground plane 208 where the ground pads 203 located along the circumference of the ground plane 208 are partially extended from the circumference of the ground plane 208, in order for the ground pads 203 as well as a portion of the surface of the dielectric layer 100 surrounding the ground pad structure 200 to be exposed from the solder mask layer 102, as shown in FIGS. 8 and 9.

Referring further to FIG. 8, the semiconductor package having a ground pad structure for preventing solder extrusion of the invention comprises: a substrate 10 having a plurality of non-ground pads 103 respectively formed on each terminal of the conductive traces 101 thereof; a ground pad structure 200 having a ground plane 208 that is made of conductive materials, and the ground plane is provided on the substrate 10 and is formed with a plurality of ground pads 203 thereon; a semiconductor chip 11 having an active surface 110 and a corresponding inactive surface 111 and being mounted on the substrate 10; a plurality of non-ground conductive metal solder means 112 and ground conductive metal solder means 112a, such as solder balls or solder bumps, and are provided on the active surface 110 of the semiconductor chip 11 in order to electrically solder the chip 11 to the corresponding non-ground pads 103 of the substrate 10 and ground pads 203 of the ground pad structure 200 in a flip-chip manner; an encapsulant body 22 encapsulating the semiconductor chip 11, the conductive metal solder means 112 and 112a, and the surface of the substrate 10; and a plurality of

conductive elements, such as solder balls 13, which are planted beneath the substrate 10.

The ground plane 208 may be disposed on the central part of the substrate 10 as shown in FIG. 8 or any other preferred location to fit a given occasion. The layout of the non-ground pads 103 and the ground pads 203 may be arranged in a matrix array as shown in FIG. 9 or any other preferred layout to fit a given occasion.

The substrate (or chip carrier) 10 may be construed by an insulative dielectric layer 100 made by insulative materials like Bismaleimide Triazine Resin, Polyimide, FR-4 Resin or FR-5 Resin, a plurality of conductive traces 101 disposed above and beneath (not shown) the dielectric layer 100, and an insulative layer, such as an insulative solder mask layer 102, which covers the conductive traces 101 and the dielectric layer 100 and has a plurality of openings 102b. The conductive traces 101 go through the substrate 10 and extend towards the top surface of the dielectric layer 100, and a plurality of non-ground pads 103 are respectively formed on each terminal of the conductive traces (not shown) on the top surface of the dielectric layer 100 and are exposed from the openings 102b of the solder mask layer 102. The other end of the conductive traces (not shown) go through the substrate 10 and extend towards the bottom surface of the dielectric layer 100, and a plurality of solder ball pads 104 are respectively formed on each terminal of the conductive traces (not shown) on the bottom surface of the dielectric layer 100 for being planted with solder balls 13.

These non-ground pads 103 may adopt the non-solder mask defined (NSMD) solder pad as shown in FIGS. 8 and 9. That is, the opening 102b of the solder mask layer 102 is larger than the solder pad 103 formed on the dielectric layer 100, and thereby expose the solder pad 103, the surface of the dielectric layer 100 surrounding the solder pad 103, and a portion of the conductive trace 101 connecting the solder pad

103 together from the opening 102b of the solder mask layer 102. Accordingly, the non-ground conductive metal solder means 112 is capable of being planted onto the solder pad 103 without contacting the solder mask layer 102 and result in a direct mounting between the surface of the dielectric layer 100 exposed around the solder pad 103 and the insulative encapsulant 12. As aforementioned, since the adhesion between the insulative encapsulant 12 and the dielectric layer 100 is good, the molten and swelled non-ground conductive metal solder means 112 due to the high reflow temperature during the reflow process for planting the solder balls will have difficulty to be extruded into the gap between the solder mask layer 102 and the dielectric layer 100 through the gap between the dielectric layer 100 surrounding the solder pad 103 and the insulative encapsulant 12. As a result, bridges occurred between the adjacent non-ground conductive metal solder means 112 or between the adjacent conductive traces 101 are well prevented.

Further, in order to overcome the occurrence of electrical shorts due to the extrusion of the molten solder means from the circumference of the ground plane toward their adjacent conductive traces, the ground pad structure 200 for preventing solder extrusion of the invention has the ground pads 203 disposed along the circumference of the ground plane 208 be formed in a non-solder mask defined manner. That is, as shown in FIGS. 8 and 9, the ground pads 203 located along the circumference of the ground plane 208 are protruded from the circumference of the ground plane 208 where the ground pads 203 located along the circumference of the ground plane 208 are partially extended from the circumference of the ground plane 208, and the ground pads 203 are exposed from the openings 102c of the solder mask layer 102. Accordingly, the outer portion of the ground conductive metal solder means 112a disposed along the circumference of the ground plane 208 is capable of being planted onto the ground pads 203 partially extended from the circumference of the ground plane 208 without contacting the solder mask layer 102 and result in a direct mounting

between the surface of the dielectric layer 100 exposed around the ground pad structure 200 and the insulative encapsulant 12. The shape of the opening 102c of the solder mask layer 102 may be formed in a doughnut shape as shown in FIG. 9 or any other preferred shape as long as the ground pads 203 as well as a portion of the surface of the dielectric layer 100 surrounding the ground pad structure 200 may be exposed from the solder mask layer 102. As a result, since the adhesion between the insulative encapsulant 12 and the dielectric layer 100 is good, the molten and swelled ground conductive metal solder means 112a due to the high reflow temperature during the reflow process for planting the solder balls will have difficulty to be extruded into the gap between the solder mask layer 102 and the dielectric layer 100 through the gap between the dielectric layer 100 surrounding the ground pads 203 located along the circumference of the ground plane 208 and the insulative encapsulant 12. As a result, bridges occurred between the adjacent conductive traces 101 are well prevented.

In addition, since the above ground pad structure 200 is capable of keeping the ground plane 208 as a complete and continuous plate-shaped plane, an excellent grounding ability is thereby well maintained.

The invention has been described using exemplary preferred embodiments. However, it is to be understood that the scope of the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements. The scope of the claims, therefore, should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.